CLAIMS

1. (Currently Amended) A semiconductor device, comprising:

conductive transfer gates comprising conductive parts;

contact plugs adjacent to said conductive transfer gates, each contact plug and each conductive transfer gate having a respective upper surface, wherein the upper surfaces of the contact plugs and the upper surfaces of the conductive parts of the transfer gates are substantially coplanar;

said each conductive transfer gate having a gate insulating film,

a gate electrode layer, and side walls for covering sides of said gate insulating film and said gate electrode layer;

a first interlayer insulating film having a surface which defines the same surface as the upper surfaces of said conductive parts of the transfer gates and said contact plugs;

a second interlayer insulating film formed on said first interlayer insulating film; and

diameter-reduced contact plugs which are smaller than said contact plugs and extend through said second interlayer insulating film to conduct to said contact plugs, respectively.

2. (Previously Amended) The semiconductor device according to claim 1, further including a memory cell section having a plurality of memory cells,

said memory cell section including, in addition to said conductive transfer gates, said contact plugs, and said first and second interlayer insulating films,

a bit line formed on said second interlayer insulating film;

a third interlayer insulating film formed on said second interlayer insulating film so as to cover said bit line; and

capacitors formed on said third interlayer insulating film;

said memory cell section further including said diameter-reduced contact plugs, which include

a bit line contact plug which extends through said second interlayer insulating film to bring said contact plugs and said bit line into conduction; and

a capacitor contact plugs which extend through said second and third interlayer insulating films to bring said contact plugs and said capacitors into conduction.

3. (Original) The semiconductor device according to claim 2, wherein said gate electrode layer has a doped silicon layer containing an impurity and a silicide film for covering the surface of the doped silicon layer,

any of said contact plugs corresponding to said capacitors, said capacitor contact plugs, and lower electrodes of said capacitors is formed of doped silicon containing an impurity,

said contact plug corresponding to the bit line has a doped silicon layer containing an impurity and a silicide film formed only at a portion brought into contact with said bit line contact plug, and

said bit line contact plug has a barrier metal brought into contact with said each contact plug and a metal layer formed on the barrier metal.

4. (Original) The semiconductor device according to claim 3, wherein said capacitor includes a capacitor insulating film formed of SiON and an upper electrode comprised of doped silicon containing an impurity.

5. (Previously Amended) The semiconductor device according to claim 2, further including a logic circuit section including a plurality of transistors, said logic section including, in addition to said transfer gates, said contact plugs, and said first and second interlayer insulating films,

bit lines formed on said second interlayer insulating film; and

said logic circuit section further including, as said diameter-reduced contact plugs,

bit line contact plugs which extend through said second interlayer insulating film to bring said contact plugs and said bit lines into conduction.

6. (Original) The semiconductor device according to claim 5, wherein said logic circuit section has NMOS transistors and PMOS transistors both of which constitute CMOS transistors.

7. (Original) The semiconductor device according to claim 6, wherein contact plugs and gate electrode layers provided in association with said NMOS transistors respectively have a doped silicon layer containing an N-type impurity, and

contact plugs and gate electrode layers provided in association with said PMOS transistors respectively have a doped silicon layer containing a P-type impurity.

8. (Original) The semiconductor device according to claim 6, wherein said memory cell section has transistors each having a first-conduction type,

one of the NMOS transistors and the PMOS transistors having a conduction type different from the first conduction type has a buried channel prepared for the first conduction type semiconductor, and a counter channel formed in a surface region of the buried channel by a semiconductor prepared for a second conduction type,

said each contact plug provided in association with the NMOS transistor has a doped silicon layer containing an N-type impurity,

said each contact plug provided in association with the PMOS transistor has a doped silicon layer containing a P-type impurity, and

any of said gate electrode layers provided in association with the NMOS transistors and said gate electrode layers provided in association with the PMOS transistors has a doped silicon layer containing a first conduction type impurity.

9. (Previously Amended) The semiconductor device according to claim 1, further including a logic circuit section including a plurality of transistors, said logic section including, in addition to said conductive transfer gates, said contact plugs, and said first and second interlayer insulating films,

bit lines formed on said second interlayer insulating film; and

said logic circuit section further including, as said diameter-reduced contact plugs,

bit line contact plugs which extend through said second interlayer insulating film to bring said contact plugs and said bit lines into conduction.

10. (Original) The semiconductor device according to claim 9, wherein said logic circuit section has NMOS transistors and PMOS transistors both of which constitute CMOS transistors.

cont C'

11. (Original) The semiconductor device according to claim 10, wherein contact plugs and gate electrode layers provided in association with said NMOS transistors respectively have a doped silicon layer containing an N-type impurity, and

contact plugs and gate electrode layers provided in association with said PMOS transistors respectively have a doped silicon layer containing a P-type impurity.

12. (Original) The semiconductor device according to claim 1, wherein said contact plugs and said gate electrode layers respectively have a doped silicon layer containing an impurity and a silicide film for covering the surface of the doped silicon layer, and

said each diameter-reduced contact plug has a barrier metal brought into contact with the silicide film, and a metal layer formed on the barrier metal.

13. (Previously Amended) The semiconductor device according to claim 1, wherein the gate electrode layer of said conductive transfer gate has a metal layer and a barrier metal which surrounds the metal layer.

Cont C1

14. (Original) The semiconductor device according to claim 1, wherein a gate oxide film of said transfer gate is a CVD insulating film formed by a CVD method.

15. (Previously Amended) The semiconductor device according to claim 1, wherein the gate insulating film of said conductive transfer gate is a thermal oxide film formed by a thermal oxidation method or a thermally-oxidized nitride film formed by a thermal oxidation nitriding method.

16-20. (Withdrawn)